EXHIBIT 26

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY TEXAS, LLC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00236
Patent 9,824,035 B2

Record of Oral Hearing
Held: April 19, 2023

Before JON M. JURGOVAN, NABEEL U. KHAN, and
KARA L. SZPONDOWSKI, *Administrative Patent Judges*.

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The above-entitled matter came on for hearing on Wednesday, April 19, 2023, commencing at 1:00 p.m. EST, by video/by telephone.

In contrast, if you look at Slide 52, Takefman does not disclose a fly-by signal topology as found in Tokuhiro. And in the absence of the fly-by distribution of the clock, and in light of the signal topology between Takefman DRAMs and the Bolt devices, clock and the D2F would arrive simultaneously at the DRAMs from the corresponding Bolt device.

In the circumstance, write leveling would be unnecessary and without any benefit. There's no motivation to use Tokuhiro's write leveling in Takefman's system as Petitioners propose. And this is a fundamental distinction that Petitioners never substantively contend with.

With respect to propagation delays that result from Takefman's architecture, Takefman discloses the use of the per-lane delay compensation circuits in Rush that we spoke about earlier, and they perform two functions; programmable launch times and lane review on receipt. The distinctions here is that Tokuhiro discloses the use of write leveling to account for different wiring links between the DRAMs and the off-module memory controller. But Takefman is arranged completely differently with no connection between Rush and the DRAMs and with each Bolt communicating with its own DRAM and Rush 301. In the absence of a fly-by distribution of clock in the command signals, write leveling, as disclosed in Tokuhiro, is wholly unnecessary. In other words, there's not a problem presented by Takefman's architecture that would be addressed by incorporating Takuhiro's write leveling that's not already addressed by Takefman's own per-lane delay compensation circuit. And again, Petitioners don't substantively address these arguments at all in their Reply.

Additionally, Dr. Przybylski provided expert testimony on how Takefman's lack of a fly-by topology affects the motivation to combine

analysis. And it's unrebutted because Dr. Albert doesn't acknowledge that distinction and hasn't offered any testimony to show why and when the distinction between the two references a POSITA would still be motivated to combine them.

And lastly I'd like to move on to the arguments relating to the obtained type of information for all grounds, unless the Board has any questions first.

If we look at Slide 55, again this is one of the logic functionalities that has to be found in the buffer circuits. The claim requires the logic to be configured to obtain timing information based on signals received by the buffer circuit during a second memory operation.

If you look at Slide 56, this is a portion of the Petition. Petitioners point only to Tokuhiro's calculation of DT2 based on delay time DT1, which is set during write leveling to disclose this claim's limitation.

If you look at Slide 57, Petitioners don't dispute a number of things. They don't dispute that Tokuhiro discloses only known write leveling procedures outlined in JESD 79C. They don't dispute that the '035 patent identified known write mechanisms as insufficient prior art. And Your Honor asked a question about that earlier. And the significance of that language in this specification is that it makes clear that if what Petitioners are pointing to to disclose this novel logic functionality that was already identified in the specification as insufficient to achieve the goals of the claims, they cannot be the same thing.

Looking at Paragraph 60 --

JUDGE SZPONDOWSKI: Counsel, isn't the memory operation described broadly in the specification though?

MS. HARGRAVE: I'm not sure that I necessarily agree that it's described broadly. I would also make very clear that the claim language here specifically relates to the second memory operation, which Petitioner has said is a write operation. So one point that's worth making is that even if, and we've included a lot of explanation and the parties have discussed, you know, quite extensively, whether or not Tokuhiro's write leveling procedure could be constituted as a memory operation.

What is undisputed is that Tokuhiro's write leveling procedure is not the write operation that Petitioners point to as the second memory operation that it has to be based upon. And you know that because for example well, let me say this also. Petitioner confessed for the first time today that the terms "write leveling" and "write operation" are synonymous. But counsel expressly conceded that in write leveling you don't have a writing of data as in a typical write manage. He acknowledged the distinction between the two things.

The Petition itself refers to write leveling and write operations distinctly. Tokuhiro also differentiates between write leveling and write operation. And so does, for that matter, the judged standard that is cited in Tokuhiro for the basis of its write leveling procedure. You know, you can see that for example if you compare the standard explanation of the write leveling procedure in Section 4.8 entitled "Write Leveling" with for example Section 4.14 which is entitled "Write Operation" with completely separate mechanisms described therein.

So even if Your Honor accepts that the specification defined memory operation broadly, what Petitioner says satisfies this claim limitation is a write operation. That's what they said the first memory operation is. And

so they can't argue tenably that write leveling and write operations are synonymous.

JUDGE KHAN: Counsel, are you saying they have not identified the write leveling operation as that first memory operation or, sorry, the second memory operation?

MS. HARGRAVE: So if you look at, yes, and I think I misspoke there. So if you look at the Petition, for example on Page 37, or let's go back. They have pointed to its other, the first memory operation, for example, on Page 29, and that portion of the Petition, they point to Osanai, and they point to the first memory operation as a write operation. I can give you a better cite here in just a minute.

But I guess the point is that in the Petition when asked to identify what that memory operation is, they don't point to write leveling at first, they point to a write operation. And now here today they seem to make the determinate that these two things are synonymous when they're not.

JUDGE KHAN: I think what they did, and I think we pointed this out in our Institution Decision, they talk about both write leveling and a write operation. But the portions of Tokuhiro that they're pointing to certainly discuss write leveling as the operation which calculates the first delay time.

MS. HARGRAVE: Yes.

JUDGE KHAN: And then I think the Petitioner is fairly explicit in their Reply that they are identifying the write leveling operation as that second memory operation. So regardless of whether or not a write operation is synonymous with the write leveling operation, I just want to make sure. Because from the papers it seems like you've understood the mapping and you have been disputing the issue of whether or not the write leveling

operation should read on a memory operation. I just actually want to clarify here it seems like Petitioner's identified the write leveling operation as a second memory operation, it seems like you understood that in your briefing. Are we consistent on that?

MS. HARGRAVE: I think the confusion here stems from the fact that, for example if you look at Claim 2. And I'd like to potentially during the break make sure that I stated this accurately. But there are portions in the Petition where they've referred expressly to a write operation. And then distinctly to write leveling operation. And so the point is that it's what they say the second memory operation is is a write operation.

I think our argument is that write leveling and write operations are not synonymous. But I understand Your Honor's point that, you know, they purportedly tried to argue that they are equivalent when they're not.

JUDGE SZPONDOWSKI: Counsel, do you dispute that a write leveling operation is a memory operation?

MS. HARGRAVE: Yes. And in fact there are substantial portions of the, you know, Response and Sur-Reply which make clear why that's the case. We pointed to the fact that nothing that is occurring during the write leveling procedure could fairly be constituted as any memory operation.

You know, I think that Petitioners today have tried to discount kind of the detail that was included about what's actually happening in Tokuhiro's write leveling procedure. But because they said for example that other operations, you know, including write commands.

But what Netlist's position has laid out very clearly in the POR is that none of the operations that occur, to the extent any operation could or any command, nothing that's happening during write leveling could fairly be

constituted as a memory operation. For example, you know, the parties don't dispute that the only thing that's happening during write leveling is these NOP and DESELECT command place holders which everyone agrees tell the memory module to do nothing. Everyone agrees that, you know, no commands other than these placeholders can be issued until the write leveling mode is exited. There's also not any dispute that the no operation placeholders are NOP commands, that the DESELECT placeholders tell the DRAM to ignore commands and address inputs.

So there seems to be no dispute that there are no memory operations performed during the write leveling procedure.

JUDGE SZPONDOWSKI: What about the write leveling procedure itself, the write leveling operation. Isn't that the memory operation?

MS. HARGRAVE: I think, no, Your Honor, it's not the memory operation. It's not a memory operation. Because again, if Petitioners are arguing that ultimately the write leveling operation is a memory operation, and ultimately what you heard Petitioners argue today is that a write leveling operation is a memory operation because it's a write operation. That's what Petitioners have argued today. They say it's a memory operation because it's a type of write operation.

And the issue is that that cannot be so based on Tokuhiro itself, which distinguishes between write leveling and write operations. And the Petition itself refers distinctly to write operations, for example, as performed in Osanai from the write leveling procedure performed in Tokuhiro. So they're distinct.

JUDGE JURGOVAN: Counsel, I have one question for you. And that is, is a memory read operation equivalent to a read leveling operation,

certainly very helpful. We will take them under advisement and issue an order in due course.

And that concludes the hearing.

(Whereupon, the proceedings at 2:58 p.m. were concluded.)

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